Docket No. NEC-F92/USA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re patent application of

Keizo Yamada

Serial No.: Not Yet Assigned

Group Art Unit: Not Yet Assigned

Filing Date: Concurrently Herewith

Examiner: Unknown

For: SEMICONDUCTOR DEVICE TEST METHOD AND SEMICONDUCTOR DEVICE TESTER

Assistant Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits and calculation of the filing fee, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claim as follows:

A1

9. (Amended) A semiconductor device tester as claimed in claim 3, wherein said comparator means includes means for integrating current flown from a rising edge to a falling edge of a current waveform generated by a certain circuit pattern on the test sample, divider means for dividing a result of integration from said integrating means by a distance between the rising edge and the falling edge of the current waveform and average value comparator means for comparing the quotient obtained by said divider.

Please add claim 25 as follows:

A2

- - 25. (New) A semiconductor device tester as claimed in claim 4, wherein said comparator means includes means for integrating current flown from a rising edge to a falling edge of a